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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/524,893	02/17/2006	Ryuichi Shimada	B-5648PCT 622443-2	5882

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EXAMINER	
AMRANY, ADI	
ART UNIT	PAPER NUMBER
2836	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/524,893	SHIMADA ET AL.	
	Examiner	Art Unit	
	ADI AMRANY	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 February 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *2/15/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The disclosure is objected to because the listing of the figures (page 7) should come before the Disclosure of the Invention (pages 3-7). See MPEP 608.01.

Appropriate correction is required.

Claim Objections

2. Claim 1 is objected to because:

a. Line 7; “its” is not entirely clear. The phrase should be written as "the AC terminal of the bridge circuit."

b. Line 15; the switch pairs are not turned on simultaneously. The last 3 lines of claim 1 clearly indicates that when one pair is on, the other is off (alternately). Claim 1 recites that the switches are not on simultaneously.

3. Claim 2 is objected to because there is no indication in the claim of what component is replenished (lines 4-5).

Appropriate correction is required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-3 and 5 are rejected under 35 U.S.C. 102(b) as being anticipated by Toyama (US 5,751,121).

With respect to claim 1, Toyama discloses a pulse power supply device (fig 1; col. 2, lines 26-33) for supplying a bipolar pulse current to an inductive load (2), wherein;

an energy source capacitor (17; col. 2, line 63 to col. 3, line 1) initially charged is connected to a DC terminal of a bridge circuit (5) composed of four inverse conductive semiconductor switches (23a-d; col. 3, lines 15-21), and the inductive load is connected to its AC terminal;

a control circuit (7, 24) for giving a control signal to gates of the switches and controlling an on/off state of the switches is provided;

the control circuit controls pairs of the switches positioned so that the pairs are turned on alternately, so that when at least one of the paired switches is on, the other paired switches are off (col. 3, lines 17-21).

The preamble of claim 1 is interpreted as an inherent result of operating the control circuit according to the limitations of claim 1. Support for this interpretation can be found in the language of the preamble: "for supplying a bipolar pulse current to an inductive load with high repetition and regenerating residual magnetic energy of a system so as to use it for next discharge." Further, claim 1 recites that the control circuit activates the switches to supply a bipolar pulse current to an inductive load. Since no other components are recited, the regeneration of magnetic energy is interpreted as an inherent result of operating the control circuit according to claim 1.

With respect to claim 2, Toyama discloses a low-voltage large-current power supply (4; col., 2 lines 34-62) is inserted in series with the load so as to replenish lost energy due to discharge so as to increase or decrease next discharge.

With respect to claims 3 and 5, Toyama discloses the switches are power MOSFETs (col. 3, lines 15-17).

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claim 1 is rejected under 35 U.S.C. 102(e) as being anticipated by Yuzurihara (US 6,760,234).

With respect to claim 1, Yuzurihara discloses a pulse power supply device (fig 1; col. 6) for supplying a bipolar pulse current to an inductive load (Lr), wherein;

an energy source capacitor (Cf1; lines 16-35) initially charged is connected to a DC terminal of a bridge circuit (13) composed of four inverse conductive semiconductor switches (Q1-4; lines 36-40), and the inductive load is connected to its AC terminal;

a control circuit (inherent; lines 41-46) for giving a control signal to gates of the switches and controlling an on/off state of the switches is provided;

the control circuit controls pairs of the switches positioned so that the pairs are turned on alternately, so that when at least one of the paired switches is on, the other paired switches are off (col. 7, lines 14-20).

With respect to claim 2, Yuzurihara discloses a low-voltage large-current power supply (40; col. 16) is inserted in series with the load so as to replenish lost energy due to discharge so as to increase or decrease next discharge.

With respect to claims 3 and 5, Yuzurihara discloses the switches are any kind of power MOSFET, inverse-conductive GTO thyristors, and units constituted so that diodes and semiconductor switches such as IGBT (col. 6, lines 41-46) and the like are connected in parallel.

With respect to claims 4 and 6-7, Yuzurihara discloses one of the two pairs of switches is replaced by diodes (d1-4; col. 6, lines 47-51). The diodes are connected in inverse-parallel with the switches, such that when a pair of switches is off, the switches are electrically "replaced" by the diodes.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 1-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Moriguchi (US 5,926,381).

With respect to claim 1, Moriguchi discloses a pulse power supply device (fig 1) for supplying a bipolar pulse current to an inductive load (52; col. 4, lines 25-38), wherein;

an energy source capacitor (16; col. 3, lines 13-19) initially charged is connected to a DC terminal of a bridge circuit (22; col. 3, line 44 to col. 4, line 24) composed of four inverse conductive semiconductor switches (28, 30, 40, 42), and the inductive load is connected to its AC terminal;

a control circuit (51) for giving a control signal to gates of the switches and controlling an on/off state of the switches is provided;

the control circuit controls pairs of the switches positioned so that the pairs are turned on alternately, so that when at least one of the paired switches is on, the other paired switches are off (fig 2a, lines (a) and (b); col. 4, line 51 to col. 5, line 26).

Moriguchi discloses the four switches are turned on/off so that only two switches (at least one of the pairs) are on at any one time (fig 2a). Further, it would be obvious to one skilled in the art to draw the schematic of figure 1, such that the switches are "positioned on diagonal lines," as the physical arrangement of the switches has no effect on their electrical switching.

With respect to claim 2, Moriguchi discloses a low-voltage large-current power supply (6; col. 2, line 57 to col. 3, line 12) is inserted in series with the inductive load so as to replenish lost energy due to discharge so as to increase or decrease next discharge current. Moriguchi discloses the boost circuit (6) recharges the capacitor (16)

to replenish lost energy (due to discharge of the capacitor) and to increase or decrease next discharge current. Moriguchi discloses the rectifier (4), boost converter (6), inverter (22) and load (52) are all in series with each other. Further, “low” voltage and “large” current are not defined in the claim. These relative terms (low/high, large/small) can be interpreted broadly.

With respect to claims 3 and 5, Moriguchi discloses the switches are any kind of power MOSFET, inverse-conductive GTO thyristors, and units constituted so that diodes and semiconductor switches such as IGBT (col. 3, lines 49-50 and 62-63) and the like are connected in parallel.

With respect to claims 4 and 6-7, Moriguchi discloses one of the two pairs of switches is replaced by diodes (32, 36, 44, 46). The diodes are connected in inverse-parallel with the switches, such that when a pair of switches is off, the switches are electrically "replaced" by the diodes.

10. Claims 4 and 6-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Toyama.

It would be obvious to one skilled in the art that a transistor, including a MOSFET, can be replaced by an equivalent circuit that includes a diode.

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ADI AMRANY whose telephone number is (571)272-0415. The examiner can normally be reached on Mon-Thurs, from 10am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Sherry can be reached on (571) 272-2800 x36. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Michael J Sherry/
Supervisory Patent Examiner, Art Unit 2836

AA